where n and m are integers.

2. (Once Amended) The crossbar device of claim 1, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transistor.

3. (Once Amended) The crossbar device of claim 1, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transistor.

5. (Once Amended) The crossbar device of claim 1, wherein the device further comprises a plurality of p to q decoder logics coupled to the input lines, where p and q are integers, with p being less than q.

7. (Once Amended) A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically associated with the memory element; and

a voltage supply structure coupled to the crossbar device designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the input voltage of the output buffers at Vdd.

8. (Once Amended) The reconfigurable circuit of claim 7, wherein at least one of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

9. (Once Amended) The reconfigurable circuit of claim 8, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transistor.

10. (Once Amended) The reconfigurable circuit of claim 8, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transistor.

11. (Once Amended) The reconfigurable circuit of claim 7, wherein each of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

15. (Once Amended) A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least an output buffer; and

a power-on circuitry coupled to the crossbar devices to force the output buffers to a known logic value at power-on.

17. (Once Amended) The reconfigurable circuit of claim 15, wherein at least one of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

18. (Once Amended) The reconfigurable circuit of claim 17, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transistor.

19. (Once Amended) The reconfigurable circuit of claim 17, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transistor.

20. (Once Amended) The reconfigurable circuit of claim 15, wherein each of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

22. (Once Amended) The reconfigurable circuit of claim 15, wherein

each crossbar device further having at least a memory element electrically associated to an output buffer; and

the reconfigurable circuit further comprises a voltage supply structure coupled to the crossbar devices designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the voltage supply of the output buffers at Vdd.

REMARKS

Summary of the Office Action

In the present application, claims 1-24 stand rejected. In addition, the drawings, specification and claims where objected to due to informalities.